REMARKS

The Examiner has rejected Claims 11-17 under 35 U.S.C. 102(b) as being anticipated by Liron, U.S. Patent No. 4,428,044. Applicant's representatives have amended most of the rejected claims, and respectfully provide the following remarks regarding Claims 11-17.

Regarding Claim 11, this claim has been amended to recite that the shared path includes a switchable component for determining which data is to be routed over the shared path. Moreover, this switchable component provides passage of data over the shared path between the two controller memory modules. The bus 217 of Liron does not provide such a switchable component, accordingly it is believed that Claim 11 is patentable.

Regarding Claim 12, note that this claim has been amended to recite that data is transferred "between said first controller memory module and said second controller memory module **using each of said direct memory access engines**".

Regarding the Examiner's rejections of Claim 12, it is respectfully requested that the Examiner identify in Liron a "second channel interface module" that is different from the "first channel interface module" of Claim 1, wherein the "second shared path" recited in Claim 12 is included therein. Additionally, it is respectfully requested that the Examiner clarify how Liron's double headed arrow 216 of Fig. 2 constitutes "a second shared path."

Regarding the Examiner's reference to the double headed arrow 216 (e.g., Fig. 2), it is respectfully noted that the double headed arrow 216 is only described in the specification as, apparently, being the pair of conductors 316 and 317 (see Liron, Fig. 9) on which clock pulses are transmitted between the master clock 301 of microcomputer 200 and the corresponding master clock of microcomputer 204 as the following passage from Liron discloses:

> "The purpose of master clock 301 is to generate the basic clock pulses required by microprocessor 300. Master clock 301 selects the output of its own internal crystal oscillator or the clock-1 signal on conductor 318. The clock-1 signal is generated by the master clock circuit in the other microcomputer of FIG. 2. This capability of master clock 301 selecting either its own internal clock oscillator or the clock-1 signal allows the generation of clock pulses to microprocessor 300 to continue should either source of clock pulses fail. Slave clock 308 is similar to master clock 301 with the following exception: it contains no internal crystal

> oscillator and selects either the clock-1 signal on conductor 318 or the clock-0 signal on conductor 317. The derived clock pulses are transmitted to microprocessor 307." (Liron, Col. 7, Ln. 23)

Applicant's representatives believe that the clock signal conductors 316 and 317 do not constitute a "second shared path" through which data passes wherein direct memory access engines are used. Accordingly, it is believed that Claim 12 is patentable both due to the reasoning provided here, as well as, due to this claim's dependence on Claim 11.

Regarding Claim 13, it is respectfully requested that the Examiner identify the passive backplane in Fig. 2 in that it is believed that no such passive backplane is shown in Fig. 2. Moreover, it is believed that no such backplane is disclosed or suggested in Liron. One description of a passive backplane is provided within the following definition of "backplane":

> (bak´plān) **(n.)** A circuit board containing sockets into which other circuit boards can be plugged in. In the context of PCs, the term backplane refers to the large circuit board that contains sockets for expansion cards.
>
> Backplanes are often described as being either *active* or ***passive***. Active backplanes contain, in addition to the sockets, logical circuitry that performs computing functions. In contrast, passive backplanes contain almost no computing circuitry.
>
> Traditionally, most PCs have used active backplanes. Indeed, the terms *motherboard* and *backplane* have been synonymous. Recently, though, there has been a move toward **passive backplanes**, with the active components such as the CPU inserted on an additional card. Passive backplanes make it easier to repair faulty components and to upgrade to new components.
> http://www.webopedia.com/TERM/B/backplane.html

Another description of "passive backplane" is as follows:

> All the active circuitry that [in] is normally found on an "active" PC motherboard (such as the CPU) is moved to a plug-in card. The new motherboard has nothing on it other than connectors, and is referred to as a **passive backplane**. The chance of a passive backplane failing is very low. Also referred to as "slot card"

technology. (8/97)

http://topcc.org/glossary/glossp.htm

As shown in the Figs. 2, 3, and 5-11 of the present application, the passive backplane 116 is a module separate from the controller memory modules 104 and 108, and additionally, is separate from the channel interface modules 136 and 140. Moreover, the passive backplane 116 provides the operative data communication paths between the controller memory modules (CMM) 104 and 108, and the memory interface modules (CIM) 136 and 140. The presence of the passive backplane 116 is important in that it allows failures of one of the memory modules 104 and 108, or the channel interface modules 136 and 140 to be replaced while the network bridge 100 is operable for storing and retrieving data. In particular, the passive backplane connections to the modules 104, 108, 136, and 140 may be disconnected while the network bridge 100 is operating for replacement of a malfunctioning module. Moreover, note that the passive backplane provides data paths for transmitting data between each pair of the modules 104, 108, 136, and 140. It is believed that a passive backplane component is not disclosed or suggested in Liron.

Regarding the Examiner's rejection of Claim 14 that Liron teaches an apparatus for sharing data between a first memory controller module and a second controller memory module, it is believed that the present claim is patentable for the reasoning provided above for the patentability of Claim 11. That is, Liron does not disclose or suggest a channel interface module having a shared path, wherein the shared path has a switchable component operably associated therewith for selecting which data is to be routed on the shared path. Accordingly, it is believed that Claim 14 is patentable.

Regarding Claim 15, it is believed this claim is patentable for similar reasoning provided hereinabove for the patentability of Claim 12. Accordingly, it is believed that Claim 15 is patentable both due to reasoning provided here, as well as, due to this claim's dependence on Claim 14.

Regarding Claim 16, it is believed this claim is patentable since Liron does not disclose or suggest a passive backplane.

Regarding Claim 17, it is believed this claim is patentable at least due to its dependence on patentable Claims 14 and 16.

NEW CLAIMS

New Claim 18 recites that "the first shared path transmits the first data between the direct memory access engines of the first and second controller memory modules". It is believed that no known prior art provides this limitation in combination with the limitations of Claim 11. Accordingly, it is believed that Claim 18 is patentable.

New Claim 19 recites providing a plurality of data buses is operably connected between a first one of the direct memory access engines and the shared path for communicating the first data. It is believed that no known prior art provides this limitation in combination with the limitations of Claim 11. Accordingly, it is believed that Claim 19 is patentable.

New Claim 20 recites providing a second plurality of data buses operably connected between a second one of the direct memory access engines, and a second shared path (as in Claim 12) for communicating second data between the first controller memory module, and the second controller memory module. It is believed that no known prior art provides this limitation in combination with the limitations of Claim 11 and 12. Accordingly, it is believed that Claim 20 is patentable.

New Claim 21 recites the second shared path (of Claim 12) having "a second switchable component for determining which data is to be routed over the second shared path". It is believed that no known prior art provides this limitation in combination with the limitations of Claim 11 and 12. Accordingly, it is believed that Claim 21 is patentable.

New Claim 22 recites the passive backplane including two data busses for communicating with each of the first and second controller memory modules. It is believed that no known prior art provides this limitation in combination with the limitations of Claim 11 and 13. Accordingly, it is believed that Claim 22 is patentable.

Since all claims are now believed to be in condition for allowance, Applicant's representatives request prompt allowance of the present application. It is believed that no fees are due with this transmittal beyond the fee of $50.00 for the addition of 2 new claims in excess of 20 claims, but in the event that any fees are due, please charge Deposit Account No. 19-1970.

Respectfully submitted

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